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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,920	09/11/2003	Raymond S. Tetrick	884.A31US2	6016

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,920	TETRICK, RAYMOND S.	
	Examiner	Art Unit	
	Reginald G. Bragdon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25 and 33-40* is/are allowed.

6)☒ Claim(s) *21-24 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 21-24 and 26-27 are objected to because of the following informalities:

As per claim 21, line 9, ", which is" should be --being--.

As per claim 21, line 10, ", which is" should be --being--.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-24 and 26-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Macon, Jr. et al. (5,600,817).

As per claim 21, Macon, Jr. et al. teaches a read-ahead ("*prefetch*") process for a mass storage ("*input/output device*") system. A portion of a cache in the main memory (DCACHE 7) is set aside as a "Most Recently Read-Ahead Section" or MRRS. The system includes a file system 10 ("*I/O control circuit*"), which may be embodied in hardware or software. See column 4, lines 43-51. The file system includes read-ahead functionality (Length 16, COMP 14, Address

12, and CONT 18) ("*a prefetch circuit to prefetch a data block into the memory in advance of a subsequent read from the I/O device*"). The address value A1 represents the "preceding address" upon which the predicted prefetch address is based (in that the read precedes the prefetching). See column 7, lines 30-32. The address value A2 (derived from A1+L, the number of units to prefetch value) represents the "predicted address", and data is prefetched for this address value. See column 7, lines 32-34. The address value A2 is stored in the MRRS. See column 7, line 36. When an next address is "demanded", the address is compared to the address (in this case A2) associated with the MRRS ("*wherein the subsequent read is tracked to determine if the subsequent read reads from the predicted address*"). See column 5, lines 11-17, and column 7, lines 37-39. Macon, Jr. et al. teaches, with reference to figure 6, that if there is a MRRS hit ("successful"; i.e. the demand address matches the value in the MRRS in step B), then further data is prefetched (step G) ("*wherein the prefetch circuit is adapted to continue prefetching in response to the subsequent read*"). Macon, Jr. et al. further teaches, with reference to figure 6, that if there is a MRRS miss ("unsuccessful", i.e. the demand address does not match the value in the MRRS in step B) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O") ("*to stop prefetching in response to the subsequent read being unsuccessful*").

As per claim 22, CONT 18 represents a state machine, and it performs the function of updating, or adjusting, the MRRS value and the length 16 value. See column 5, lines 20-47.

As per claim 23, the read ahead functionality is located within the file system 10 which corresponds to the claimed "*I/O control circuit*" as detailed above.

As per claim 24, the file system, in which the read ahead functionality resides, is an interface for main memory 3, CPU 2, and mass storage 4.

As per claim 26, Macon, Jr. et al. teaches, with reference to figure 6, that as long as there is a first hit in the MRRS (step "B", where the address value in the MRRS is the predicted address and a hit represents the demand address matching the address in the MRRS as set forth in column 5, lines 48-50), then prefetching of a number L of units continues (step "G").

As per claim 27, Macon, Jr. et al. teaches, with reference to figure 6, that if there is a MRRS miss (i.e. the demand address does not match the value in the MRRS) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O").

As per claim 28, Macon, Jr. et al. teaches a CPU 2 ("*a processor*") and a mass storage 4 ("*an Input/Output (I/O) device*"). The system includes a file system 10, which may be embodied in hardware or software. See column 4, lines 43-51. The file system includes read-ahead functionality (Length 16, COMP 14, Address 12, and CONT 18). The address value A1 represents the "preceding address" upon which the predicted prefetch address is based (in that the read precedes the prefetching). See column 7, lines 30-32. The address value A2 (derived from A1+L, the number of units to prefetch value) is used to prefetch data ("*the prefetch interface predicts an address needed within the I/O device to satisfy the request*"). See column 7, lines 32-34. The address value A2 is stored in the MRRS. See column 7, line 36. When an next address is "demanded", the address is compared to the address (in this case A2) associated with the MRRS ("*the prefetch interface tracks its performance*"). See column 5, lines 11-17, and column 7, lines 37-39. Macon, Jr. et al. teaches, with reference to figure 6, that as long as there is a first hit in the MRRS (step "B", where the address value in the MRRS is the predicted address and a hit represents the demand address matching the address in the MRRS as set forth in column 5, lines 48-50), then prefetching of a number L of units continues (step "G")

("*performs, in response to success rates, continuing to prefetch for additional data for favorable success rates*"). Macon, Jr. et al. further teaches, with reference to figure 6, that if there is a MRRS miss (i.e. the demand address does not match the value in the MRRS) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O") ("*performs, in response to success rates, ... and stopping prefetching for the additional data for unfavorable success rates*"). The MRRS is representative of prior prefetched data (most recently read ahead section), where a first hit in the MRRS results in further prefetching.

As per claim 29, Macon, Jr. et al. teaches that the entire address value in the MRRS must match the demand value (column 5, lines 48-50). Therefore, "at least a portion of the prefetched data" satisfies the request.

As per claim 30, as set forth in figure 6, the prefetching is configured to adjust whether or not to prefetch, and how much to prefetch (the L value) based on hits or misses in the MRRS and Dcache.

As per claim 31, CONT 18 represents a state machine, and it performs the function of updating, or adjusting, the MRRS value and the length 16 value. See column 5, lines 20-47.

As per claim 32, CONT 18 controls whether prefetching occurs (i.e. step G of figure 6 is performed) or does not occur (step G is not performed). See figure 6.

Allowable Subject Matter

4. Claims 25 and 33-40 are allowed.

Response to Arguments

5. Applicant's arguments filed 22 September 2005 have been fully considered but they are not persuasive.

Applicant has amended claims 21 and 28 to set forth both a continued prefetching operation in response to a successful prediction, and a stop prefetching operation in response to an unsuccessful prediction. However, both of these operations are taught by Macon, Jr. et al. as set forth above in the rejection of the claims under 35 U.S.C. 102.

Applicant also argues that step N shows that a prefetch always occurs and that data is located in the DCACHE is always prefetched data. This is not accurate. Step N sets forth "fetching" data, i.e. demand data. This is not a prefetch operation. While step N leads to a prefetch operation (step G), at any point in time there is no guarantee that data being accessed in the cache was placed in the cache as a result of a prefetch. The transition from I to J could take place because of a hit on "demand" data fetched in step N is located in the cache, not "prefetch" data from step G.

Second, figure 6 clearly shows an example where a demand to the system does not result in a prefetch (steps A, B, I, J, K). The fact that steps N-G may have been performed in the past to place data in the cache does not indicate that steps N-G have been performed for the current access.

Finally, it is not clear how Applicant's remarks that Macon, Jr. et al. "always performs at least one prefetch for a given entry"(emphasis added) (page 6 of the response filed 20 May 2005; page 8 of the response filed 22 September 2005) relates to any language in claims 21 and 28.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(571) 273-8300**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(571) 273-4204**, only after approval by the Examiner.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (571) 272-4210.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2185

RGB
December 12, 2005